# Design Implementation Plan – 1 TH/s ASIC Mining Chip

This document outlines the comprehensive design implementation plan for a 1 TH/s cryptocurrency mining ASIC targeting the open‑source SKY130 130 nm CMOS process. The plan breaks the development process into detailed phases, identifying key activities, tools/techniques, and tangible deliverables at each step.

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| --- | --- | --- | --- |
| Phase | Sub‑Tasks / Description | Tools / Techniques | Deliverables |
| 1. Requirements & Planning | - Define hash algorithm (SHA‑256) - Set power/area/throughput targets - Draft architecture style (pipeline hierarchy) | Documentation, Analysis | Architecture Specification, Block Diagram |
| 2. System‑Level Design | - High‑level block diagram - Partition core vs. control logic - Define bus/interconnect schemes | Draw.io, SystemVerilog planning, spreadsheets | System Architecture Spec, Interface Definitions |
| 3. RTL Microarchitecture | - RTL for grand/child/grandchild modules - FSMs, datapaths, pipelining - Power‑aware RTL (clock gating) | Verilog / SystemVerilog | RTL Code, Module Descriptions |
| 4. RTL Functional Verification | - Develop testbenches (unit & integration) - Coverage analysis & regression runs | Icarus Verilog, Verilator, ModelSim, SVTB | Simulation Logs, Coverage Reports |
| 5. Timing Constraint Development | - Define clock constraints, I/O delays - Identify multicycle & false paths | SDC format, STA methodology | Constraints File (SDC) |
| 6. Synthesis | - RTL → gate‑level netlist - Optimize for area, power, timing | Yosys, ABC | Synthesized Netlist, Reports |
| 7. Floorplanning | - Define die/core area (28 × 28 mm) - Place top‑level blocks and macros | OpenROAD, custom scripts | Floorplan DEF, Power Plan Overview |
| 8. Power Network Design | - Generate power rings/straps - Insert decoupling caps (decaps) - Verify power domains | OpenROAD, Magic | Power Distribution Network Layout |
| 9. Placement | - Standard‑cell placement - Density and legalization checks | OpenROAD placer | Placed Netlist DEF |
| 10. Clock Tree Synthesis (CTS) | - Generate balanced clock tree - Insert clock gating cells | OpenROAD CTS | Clock Tree DEF, Skew Reports |
| 11. Routing | - Global & detailed routing - Shield critical nets & fix DRC | OpenROAD router | Routed Layout DEF |
| 12. Physical Verification (DRC/LVS) | - Run DRC - Perform LVS & antenna checks | Magic, Netgen, KLayout | DRC/LVS Clean Layout |
| 13. Parasitic Extraction (PEX) | - Extract RC parasitics - Prepare SPEF for STA | Magic, SPEF generation | SPEF Files, Annotated Netlist |
| 14. Static Timing Analysis | - Verify timing closure across PVT corners - Analyze setup/hold and clock uncertainty | OpenSTA | STA Reports |
| 15. Gate‑Level Simulation | - Post‑synthesis & post‑route sims with SDF - Validate functional equivalence | Verilator + SDF | Back‑Annotated Simulation Logs |
| 16. Power Analysis & Optimization | - Vector‑based dynamic power analysis - Identify hotspots & optimize | Activity file generation, clock gating refinement | Final Power Report |
| 17. Formal Equivalence Checking | - Ensure gate‑level ≡ RTL behavior | Open‑source/commercial formal tools | Pass/Fail Report |
| 18. GDSII Generation | - Export final layout for fabrication - Integrate frame, alignment, and label cells | OpenROAD, Magic | Final GDSII File |
| 19. Documentation & Review | - Maintain specs, build instructions - Conduct design reviews & audits | Markdown, Git, LaTeX | Design Docs, Review Reports |
| 20. Tape‑out Preparation | - Validate GDSII & sign‑off data - Assemble fab checklist & manifest | GDSII sign‑off checklist | Tape‑out Package |
| 21. Post‑Silicon Validation Plan | - Develop silicon test strategy - Plan board bring‑up & characterization | Bench tools, JTAG, on‑chip debug | Validation Plan, Test Vectors |

Project Schedule – 1 TH/s ASIC Mining Chip

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| --- | --- | --- | --- |
| Phase | Start Date | End Date | Duration (Days) |
| Requirements & Planning | 2025-07-10 | 2025-07-13 | 4 |
| System-Level Design | 2025-07-14 | 2025-07-18 | 5 |
| RTL Microarchitecture | 2025-07-19 | 2025-07-24 | 6 |
| RTL Functional Verification | 2025-07-25 | 2025-07-30 | 6 |
| Timing Constraint Development | 2025-07-31 | 2025-08-02 | 3 |
| Synthesis | 2025-08-03 | 2025-08-07 | 5 |
| Floorplanning | 2025-08-08 | 2025-08-11 | 4 |
| Power Network Design | 2025-08-12 | 2025-08-15 | 4 |
| Placement | 2025-08-16 | 2025-08-19 | 4 |
| Clock Tree Synthesis (CTS) | 2025-08-20 | 2025-08-23 | 4 |
| Routing | 2025-08-24 | 2025-08-28 | 5 |
| Physical Verification (DRC/LVS) | 2025-08-29 | 2025-09-02 | 5 |
| Parasitic Extraction (PEX) | 2025-09-03 | 2025-09-06 | 4 |
| Static Timing Analysis | 2025-09-07 | 2025-09-09 | 3 |
| Gate-Level Simulation | 2025-09-10 | 2025-09-12 | 3 |
| Power Analysis & Optimization | 2025-09-13 | 2025-09-17 | 5 |
| Formal Equivalence Checking | 2025-09-18 | 2025-09-20 | 3 |
| GDSII Generation | 2025-09-21 | 2025-09-22 | 2 |
| Documentation & Review | 2025-09-23 | 2025-09-25 | 3 |
| Tape-out Preparation | 2025-09-26 | 2025-09-28 | 3 |
| Post-Silicon Validation Plan | 2025-09-29 | 2025-10-02 | 4 |

# Fabrication Plan – 1 TH/s ASIC Mining Chip

This section outlines the plan for fabrication of the 1 TH/s ASIC Mining Chip using the open-source SKY130 PDK. Fabrication requires close coordination with a foundry capable of processing the SKY130 design, ensuring proper GDSII validation, documentation, and submission packaging.

## 1. Fabrication Partner & Foundry

- Use a partner foundry that supports the SKY130 process (e.g., SkyWater Technology).  
- Confirm compatibility with GDSII design rule set and submission process.  
- Coordinate tapeout slots and logistics.

## 2. Tapeout Checklist

- Final GDSII file with verified DRC and LVS.  
- Netlist (Verilog), LEF/DEF files, and parasitic SPEF files.  
- Floorplan and layout documentation.  
- Timing, power, and area reports.  
- Signed-off SDC constraints.  
- README or manifest documenting tool versions and process steps.  
- Checklist of IP usage and licensing compliance.

## 3. Submission Process

- Package GDSII and supporting data into a verified format as required by the foundry.  
- Submit to the fabrication partner via their secure portal or protocol.  
- Maintain versioned backup of submitted files.  
- Track confirmation of submission and expected fabrication timeline.

## 4. Mask Generation & Fabrication Timeline

- After submission, allow time for mask generation (1–2 weeks).  
- Actual wafer fabrication may take 8–12 weeks depending on foundry schedule.  
- Allow additional time for packaging and delivery.

## 5. Post-Fabrication Activities

- Receive packaged dies and perform initial bring-up tests.  
- Validate hash computation functionality on silicon.  
- Perform power and performance benchmarking.  
- Identify any silicon bugs and log for future tapeout iterations.

# Costing Plan – Up to Packaging

The following table outlines the estimated cost breakdown for the complete ASIC development process, from RTL design to final chip packaging. The costs are based on open-source tools where possible and industry-average fabrication and packaging fees for SKY130-compatible foundries.

|  |  |  |  |
| --- | --- | --- | --- |
| Category | Item | Estimated Cost (USD) | Remarks |
| Design & Verification | EDA Tools (open-source) | 0 | Using Yosys, OpenROAD, Magic, Verilator |
| Design & Verification | Workstation Hardware | 2,500 | High-performance workstation for synthesis and layout |
| Design & Verification | Man-hours for RTL/PD | 30,000 | Assuming small engineering team over 4–5 months |
| Verification | Regression Simulations | 2,000 | Compute resource costs |
| Tapeout Preparation | DRC/LVS/STA Tools | 0 | Open-source (Magic, OpenSTA) |
| Fabrication | GDSII Submission | 5,000 | GDSII verification and submission fees |
| Fabrication | Mask Set (MPW run) | 10,000 | Multi-Project Wafer run with SkyWater |
| Fabrication | Wafer Fabrication | 15,000 | Approx. cost for fabrication of 40–50 dies |
| Packaging | Chip Packaging (QFN/BGA) | 5,000 | Low-cost plastic packaging for initial test batch |
| Logistics | Shipping and Handling | 1,000 | Packaging, customs, and delivery |

\*\*Total Estimated Cost (USD):\*\* $70,500